36 (Added). The electronic structure of claim 32 wherein the circuit lines are about 5 to about 20 microns thick.

37 (Added). The electronic structure of claim 32 wherein the circuit lines are 5 to about 10 microns thick.

38. An electronic structure which comprises at least two of the structures of claim 32 stacked together.

## REMARKS/ARGUMENTS

Claims 1, 3-11 and 18-38 are now in the application. Claims 1, 3-11 and 32-38 are directed to the elected invention. Claims 11 and 18-31 are drawn to non-elected inventions and may be cancelled by the Examiner upon the allowance of the claims directed to the elected invention. Claim 1 has been amended to include recitations from prior claim 2. Newly presented independent claim 32 includes recitations from claims 1, 3 and 5.

Attached are proposed drawing changes as requested by the Examiner.

The rejections of claims 1and 5-6 under 35 USC 102(b) as being anticipated by U.S. Patent 5,620,800 to Leeuw and of claims 1 and 10 under 35 USC 103(a) as being unpatentable over US Patent 3,324,014 to Modjeska and US Patent 3,149,265 to Thorn, US Patent 4,875,282 to Leibowitz and US Patent 5,004,640 to Nakatani have been rendered moot by the amendments to claim 1 including recitations from claim 2, since claim 2 was not rejected under these references.

Claims 1-4 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 4,306,925 to Lebow et al. and claims 7-10 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 4,306,925 to Lebow et al (hereinafter also referred to as "Lebow"). Lebow fails to anticipate or render obvious these claims.

The present invention provides for obtaining a structure having dense embedded flush circuitry features. The present invention makes it possible to create circuitry features that are much more densely configured than those fabricated using current methods. This

is made possible since the final structure is a circuitry feature having dielectric regions and conductive features that are coplanar.

In particular, the present invention relates to a structure comprising a first dielectric layer of a polymeric material having a first top surface; a second dielectric layer of polymeric material on the first top surface of the first dielectric layer of a polymeric material, having a second top surface, the second layer of polymeric material also having trench features therein; electrically conductive material deposited in said trench features forming electrically conductive circuit lines and being substantially flush with the second top surface of the second dielectric layer of polymeric material.

Moreover, the structure of claim 1 and claims dependent thereon include a third dielectric layer of polymeric material located on the electrically conductive circuit lines.

The present invention is especially advantageous for fabricating buried interconnection levels that are in close proximity to one another in a printed circuit board structure.

As discussed in the specification, printed circuit board interconnection levels prior to the present invention are built on top of a dielectric thin film layer. Circuitry features are formed using photolithographic and subtractive etch techniques. In a typical method, a metallic foil and especially copper foil is laminated to the substrate followed by using photolithographic and subtractive etching to create the circuitry. The copper foil includes a roughened or dendritic backside surface for inducing mechanical adhesion to the substrate. Smooth copper layers do not adequately bond without an auxiliary bonding agent.

Great difficulties exist in adequately etching dendrites especially when dealing with small spaces. Moreover, along with the concern created by dendrites, the width of the lines (e.g. about 0.5 mils wide), and photolithographic issues (e.g. resolution of fine features, 0.7 mil wire with 1.1 mil space, in a thin photo resist film), and subtractive etch undercut/pad rounding, render clearly and fully resolving small line spaces such as the 1.8 mil pitch features presently desired very difficult. Additionally, this subtractive etch

approach results in unprotected circuitry features referred to as "skyscrapers" that extend above an underlying plane of dielectric barrier material.

In many structures, it is important to plate another metal such as gold or nickel-gold onto the copper circuitry. The "skyscraper" structure causes a problem of bridging or shorting between lines especially where there exist closely spaced fingers.

As discussed in the specification, the present invention addresses these concerns of the prior art.

Lebow fails to anticipate claim 1 and claims dependent thereon since, among other things, Lebow does not suggest the third dielectric layer located on the electrically conductive circuit lines. Numeral 48 in Fig. 3 of Lebow refers to a resist material which is not on the circuit lines 20 but instead is located on a layer of copper and on the insulator layer. Moreover, Figs. 1 and 3 relate to temporary structures that are subsequently converted to the desired circuitry. For instance, resist layers 18 and 22 in Fig. 1 are removed in subsequent steps.

Claims 7-11 are patentable for at least those reasons as to why claim 1 is patentable.

Claim 32 and claims dependent thereon are further patentable since claim 32 includes recitations from claim 5 which was not rejected over Lebow.

Lebow does not anticipate the present invention.

Concerning the rejections under 35 USC 102, the cited references do not disclose each and every recitation of the claimed invention. Therefore, such do not anticipate the present invention.

In particular, anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims. See *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985), *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 1 USPQ2d

1081 (Fed. Cir. 1986), and *Akzo N.V. v. U.S. International Trade Commissioner*, 1 USPQ2d 1241 (Fed. Cir. 1986).

There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 USC 102. See *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (CAFC 1991) and *Studiengesellschaft Kohle GmbH v. Dart Industries*, 220 USPQ 841 (CAFC 1984).

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, consideration and allowance are, therefore, respectfully solicited.

In the event that the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Commissioner is hereby authorized to charge any fees or credit any overpayment associated with this communication including any extension fees to Deposit Account No. 22-0185.

Dated: 12-11-02

Respectfully submitted,

By _____

Burton A. Amernick
Registration No.: 24,852
CONNOLLY BOVE LODGE & HUTZ, LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorneys for Applicant

OIPE JC48
DEC 13 2002
PATENT & TRADEMARK OFFICE

**Version With Markings to Show Changes Made**

1. (Twice Amended) An electronic structure comprising:

a first dielectric layer of polymeric material having a first top surface;

a second dielectric layer of polymeric material on said first top surface of said first dielectric layer of polymeric material, having a second top surface, said second layer of polymeric material also having trench features therein; and electrically conductive material deposited in said trench features forming electrically conductive circuit lines being substantially flush with said second top surface of said second dielectric layer of polymeric material, wherein said polymeric material is at least one member selected from the group consisting of thermoplastic resin and thermosetting resin, and further including a third dielectric layer of polymeric material located on said electrically conductive circuit lines.

OIPE JC48
DEC 13 2002
PATENT & TRADEMARK OFFICE

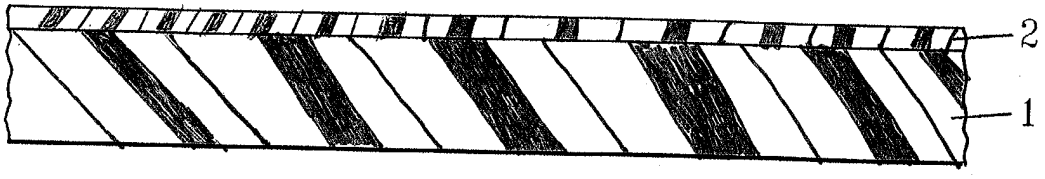


FIG. 1a

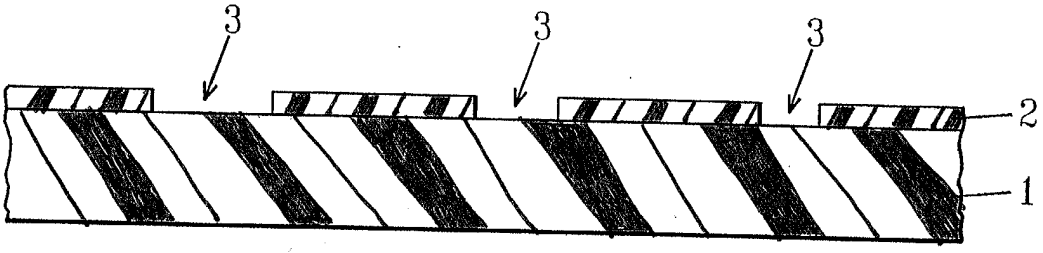


FIG. 1b

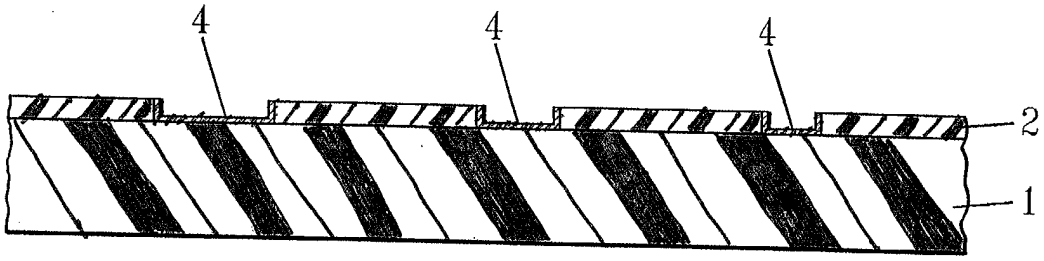


FIG. 1c

OIPE JC48
DEC 13 2002
PATENT & TRADEMARK OFFICE

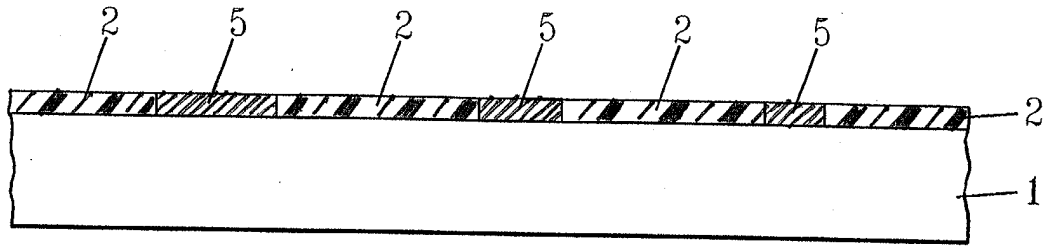


FIG. 1d

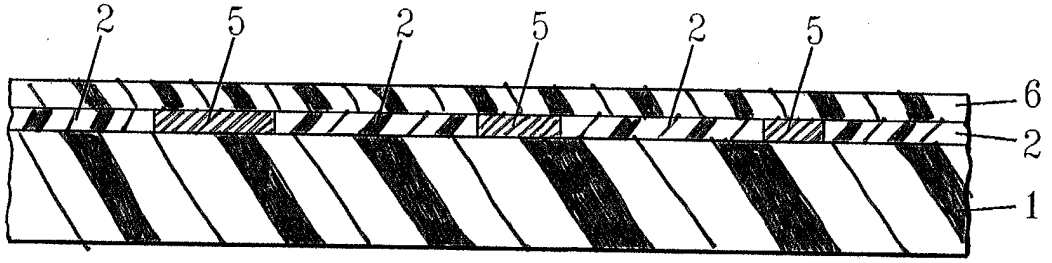


FIG. 1e